

Application No. 10/730996

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CLMPTO

1. (Currently Amended) A self-aligned inner gate recess channel in a semiconductor substrate, comprising:
  - a. a recess trench formed in an active region of the substrate;
  - b. a gate dielectric layer formed on a bottom portion of the recess trench;
  - c. recess inner sidewall spacers formed on sidewalls of the recess trench;
  - d. a gate formed in the recess trench so that an upper portion of the gate protrudes above an upper surface of the substrate, wherein a thickness of the recess inner sidewall spacers causes a center portion of the gate to have a smaller width than the protruding upper portion and a lower portion of the gate;
  - e. a gate mask formed on the gate layer;
  - f. gate sidewall spacers formed on the protruding upper portion of gate and the gate mask; and
  - g. a source/drain region formed in the active region of the substrate adjacent the gate sidewall ~~spacers~~-spacers, the recess inner sidewall spacers extending below an upper surface of the substrate a majority of a distance that the source/drain region extends below the upper surface and only a portion of a distance that the gate extends below the upper surface, and being sandwiched between the source/drain region and the gate.

2. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess trench has a width at an opening thereof of about 900 Å.

3. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess trench has a depth of between about 1300 - 1800 Å.

4. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the substrate comprises:

a shallow trench isolation region; and

the active region includes a well region, a threshold voltage control region, and a source/drain region.

5. (Original) The self-aligned inner gate recess channel as claimed in claim 4, wherein the shallow trench isolation region has a depth of approximately 3000 Å.

6. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate dielectric layer is selected from the group consisting of an oxide layer, an oxynitride layer, an alumina ( $\text{Al}_2\text{O}_3$ ) layer, and a ruthenium oxide (RuO) layer.

7. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate dielectric has a thickness of about 50 Å.

8. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess inner sidewall spacers have a thickness of about 200 Å.

9. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the recess inner sidewall spacers are formed of either silicon oxide or silicon nitride.

10. (Original) The self-aligned inner gate recess channel as claimed in claim 1, wherein the gate formed in the recess trench comprises:  
a first gate layer formed in a bottom portion of the recess trench; and  
a second gate layer formed on the first gate layer in an upper portion of the recess trench, the second gate layer having a lower portion within the recess trench and an upper portion that protrudes above the upper surface of the substrate,

wherein a thickness of the recess inner sidewall spacers causes the lower portion of the second gate layer to have a smaller width than the protruding upper portion of the second gate layer and the first gate layer.

11. (Original) The self-aligned inner gate recess channel as claimed in claim 10, wherein the first gate layer is a poly gate layer.

12. (Original) The self-aligned inner gate recess channel as claimed in claim 10, wherein the first gate layer has a thickness of about 800 Å.

13. (Original) The self-aligned inner gate recess channel as claimed in claim 10,  
wherein the second gate layer is a poly gate layer.

14. (Original) The self-aligned inner gate recess channel as claimed in claim 1,  
wherein the source/drain region in the active region of the substrate is an  $n^+$  source/drain region.

CLAIMS 15-63 (CANCELLED)